ABSTRACT OF THE DISCLOSURE

[0023] In an embodiment, a functional unit including a compressor section and a 36-bit SIMD adder is used to perform a SIMD four-pixel averaging instruction. The functional unit generates four four-pixel averages. Four pixel values and a rounding value are compressed into a sum and a carry vector. The tow least significant bits of the sum vector and the LSB of the carry vector are dropped before being input to the 36-bit SIMD adder. The two resultant 8-bit vectors are added by the 36-bit adder to directly generate the average pixel value result.